

**WHAT IS CLAIMED IS:**

1           1.     A system, comprising:  
 2           first circuitry in a first clock domain operable at a first clock frequency;  
 3           second circuitry in a second clock domain operable at a second clock  
 4 frequency;  
 5           first and second jitter buffer pairs interfacing between said first circuitry and  
 6 said second circuitry domain, said first jitter buffer pair comprising first and second  
 7 jitter buffers, and said second jitter buffer pair comprising third and fourth jitter  
 8 buffers;  
 9           wherein said first or second jitter buffers and said third or fourth jitter buffers  
 10 alternately fill at said first clock frequency and empty at said second clock frequency,  
 11 wherein alternation between said first and second jitter buffers and said third and  
 12 fourth jitter buffers occurs at said second clocking frequency.

1           2.     A system in accordance with claim 1, said first circuitry comprising an  
 2 audio input, said second circuitry comprising an encoder.

1           3.     A system in accordance with claim 1, said first circuitry comprising an  
 2 audio output, said second circuitry comprising a decoder.

1           4.     A system in accordance with claim 2, said first clock frequency  
 2 comprising a sample clock, said second clock frequency comprising a frame clock.

1           5.     A telecommunication system, comprising:  
 2 an audio input;  
 3 an audio output;  
 4 interface circuitry comprising first and second jitter buffers operably coupling  
 5 said audio input to a voice encoder and third and fourth jitter buffers operably  
 6 coupling said audio output to a voice decoder;  
 7           wherein said first or second jitter buffers alternately fill at a first clock  
 8 frequency and empty at a second clock frequency, wherein alternation between said  
 9 first and second jitter buffers occurs at said second clock frequency; and

10 wherein said third or fourth jitter buffers alternately fill at said second clock  
 11 frequency and empty at said first clock frequency, wherein alternation between said  
 12 third and fourth jitter buffers occurs at said second clock frequency.

1 6. A system in accordance with claim 5, said interface circuitry comprising  
 2 one or more digital signal processors.

1 7. A system in accordance with claim 6, said first clocking frequency  
 2 comprising a PCM sample clock frequency.

1 8. A system in accordance with claim 7, said second clock frequency  
 2 comprising a frame clock frequency.

1 9. A system in accordance with claim 8, wherein a frame comprises 160  
 2 samples.

1 10. A system in accordance with claim 9, wherein a size of said first,  
 2 second, third, and fourth buffers is 165 samples.

1 11. A method for rate adjustment using first and second jitter buffers, said  
 2 first and second jitter buffers adapted to receive a plurality of samples at a first clock  
 3 rate and transmit a block of said samples at a second clock rate, comprising:  
 4 switching between using said first or second jitter buffers at said second clock  
 5 rate.

1 12. A method in accordance with claim 11, further including third and  
 2 fourth jitter buffers, adapted to receive blocks of samples at said second clock rate  
 3 and transmit a plurality of samples at said first clock rate, comprising:  
 4 switching between using said third or fourth jitter buffers at said second clock  
 5 rate.

1        13.    A method for rate adjustment, comprising:  
 2        receiving at first or second jitter buffers a plurality of samples at a first clock  
 3 rate and transmit a block of said samples at a second clock rate; and  
 4        switching between using said first or second jitter buffers at said second clock  
 5 rate.

1        14.    A method in accordance with claim 13, further comprising:  
 2        receiving at third or fourth jitter buffers blocks of samples at said second clock  
 3 rate and transmitting a plurality of samples at said first clock rate; and  
 4        switching between using said third or fourth jitter buffers at said second clock  
 5 rate.

1        15.    A method, comprising:  
 2        providing first circuitry in a first clock domain operable at a first clock  
 3 frequency;  
 4        providing second circuitry in a second clock domain operable at a second  
 5 clock frequency;  
 6        providing first and second jitter buffers interfacing between said first circuitry  
 7 and said second circuitry domain;  
 8        wherein said first or second jitter buffers alternately fill at said first clock  
 9 frequency and empty at said second clock frequency, wherein alternation between  
 10 said first and second jitter buffers occurs at said second clocking frequency.

1        16.    A method in accordance with claim 15, said first circuitry comprising an  
 2 audio input, said second circuitry comprising an encoder.

1        17.    A method in accordance with claim 15, said first circuitry comprising an  
 2 audio output, said second circuitry comprising a decoder.

1        18.    A method in accordance with claim 16, said first clock frequency  
 2 comprising a sample clock, said second clock frequency comprising a frame clock.

